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REPORT

Pulse code modulation of video signals: parallel-to-serial and serial-to-parallel conversion

No. 1971/14

Research Department, Engineering Division
THE BRITISH BROADCASTING CORPORATION

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It uses SI units in accordance with B.S. document PD 5686.

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Summary

This report describes a method by which several streams of high-speed digits may be multiplexed together in the time domain to form a single digit stream; in particular, this method is intended to be used to combine the parallel output signals from a video a.d.c. so that they may be sent down a single link. The report also describes a method of reconverting the digits into the parallel form, which could be used at a receiving terminal before the digits are fed to a d.a.c. Equipment performing both of these functions has been constructed and tested; the resulting hardware, which used standard integrated circuits, worked well and required little initial setting up.

1. Introduction

A previous report[1] described an eight-bit analogue-to-digital converter, a.d.c., for video signals. This, as originally designed, was intended to work back-to-back with a digital-to-analogue converter, d.a.c., and the eight digits came out on eight separate wires. Later, it was necessary to carry out various tests on the effect of digital errors, as well as a digital link trial, to which end the eight outputs, together with a ninth bit used for parity checking, had to be combined into a single serial bit stream and subsequently separated for decoding. This report describes the parallel-to-serial converter, p.s.c., and the serial-to-parallel converter, s.p.c., developed for the purpose.

The p.s.c. and s.p.c. described were intended primarily for laboratory work in which the sending and receiving terminals were contiguous so that word framing information could be carried synchronously on a second wire between the two units. Eventually, framing information could be inserted into the parallel data and the extra wire will then not be required.

2. The parallel-to-serial converter

The video a.d.c. has eight outputs, each of which has a bit rate of 13·3 Mb/s. When a parity digit is added and the nine bit streams are combined together, the total data rate becomes 120 Mb/s. If this data is to be time-division-multiplexed into a single bit stream, the individual bits will occupy extremely short periods of time, approx. 8 ns. The circuits which accomplish this must be so designed that incidental delays do not affect the uniformity of the serial digit stream emerging from the p.s.c.

Two methods of parallel-to-serial conversion were tried. The first method involved sampling the input data sequentially and passing this information straight out to line. This required extremely accurate timing of the incoming data relative to the sampling pulses and the generation of the latter was difficult due in part to unavoidable delays in the internal connections. To circumvent these problems, a second method was adopted in which the inputs are all sampled simultaneously, applied to a shift register and clocked out to line sequentially. The latter solution will be described in greater detail.

A block diagram of the p.s.c. is shown in Fig. 1. The incoming data is clocked at 13·3 MHz into input latches, thus removing any amplitude variations or timing jitter that may be present on the input. The outputs from the latches are applied to gates; these gates also receive 13·3 MHz "set" pulses of 4 ns duration which are generated from the 13·3 MHz and 120 MHz clocks. The use of both clocks ensures that the "set" pulses

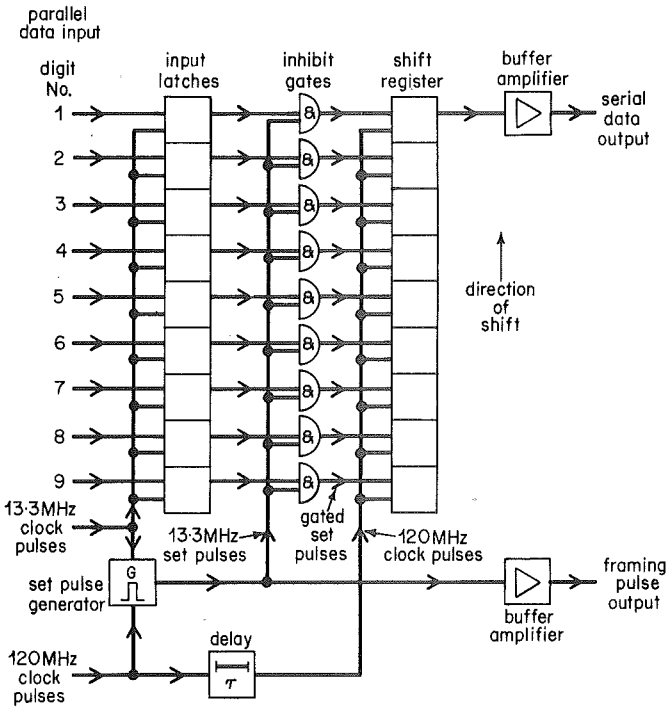

Fig. 1 - Block diagram of the parallel-to-serial converter

occur at exactly the right instant with respect to the clock pulses fed to the shift register. The outputs from the gates set new data into the shift register. Once it is there it can be clocked out serially at a rate of 120 MHz through a buffer amplifier to line. As one word of data is being clocked out at one end of the shift register, a string of "zeros" is being clocked in at the other, so that when a new data word is ready to be set into the shift register, the latter contains all zeros. Thus only the binary ones of each new word have to be set up.

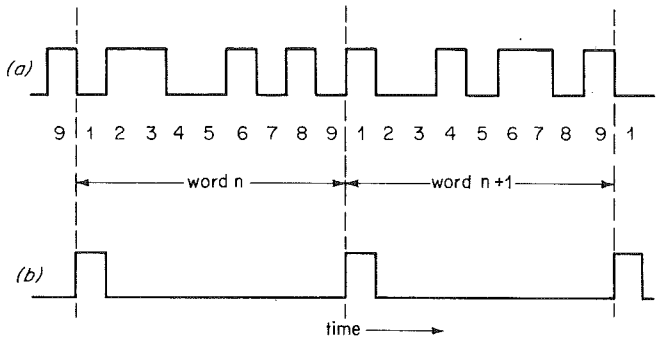

Fig. 2 - Output from parallel-to-serial converter: timing diagram
(*a*) Serial data stream (*b*) 13·3 MHz framing pulses

The form of the serial output is illustrated in Fig. 2*a*. This shows two complete digital words as they will appear out of the shift register. It will be noticed that digit number nine of word n is followed immediately by digit number one of word n + 1. Thus, as one word leaves the shift register, another must be ready to follow it immediately; there is no extra time slot during which fresh data can be set up. For this reason the gated set pulses must arrive at the shift register at a time which will present the change in data to the output of each stage just as if it had been clocked through from the previous stage. The delay through each shift register stage, from gated set pulse input to data output, is the same as the delay from clock pulse input to data output; thus the above condition can be met by ensuring that the gated set pulses arrive at the shift register in synchronism with the leading edge of clock pulses. This is achieved by using the leading edge of the 120 MHz clock pulse in the generation of the set pulses and by introducing into the path of the 120 MHz clock pulse a delay, τ, equal to the delay through the set pulse generator and the inhibiting gates.

Thus the sequence in which pulses arrive at the shift register is as follows:

Set pulses are sent to the shift register to arrive simultaneously with every ninth clock pulse. If the incoming data requires that a zero is set up in one stage of the register it inhibits the set pulse to that stage and the clock pulse clocks in a zero. Where a one is required the set pulse reaches the shift register, overrides the clock pulse, (which consequently does not need inhibiting), and sets up a one. This new word is then clocked along and out of the shift register by the next eight clock pulses.

To enable the first digit of each word to be recognised from the serial stream of digits, the set pulse which inserted the word into the shift register is passed through a second buffer amplifier and fed out in synchronism with the appropriate data digit as a 13·3 MHz framing pulse – see Fig. 2*b*. Eventually, as already stated, framing information could be inserted into the parallel data stream and the extra output would then not be required; for the intended purposes, however, this refinement was not necessary.

3. The serial-to-parallel converter

The s.p.c., Fig. 3, makes use of the time coincidence between the framing pulses and the first digit in each word in the serial stream, Figs. 2*a* and *b*.

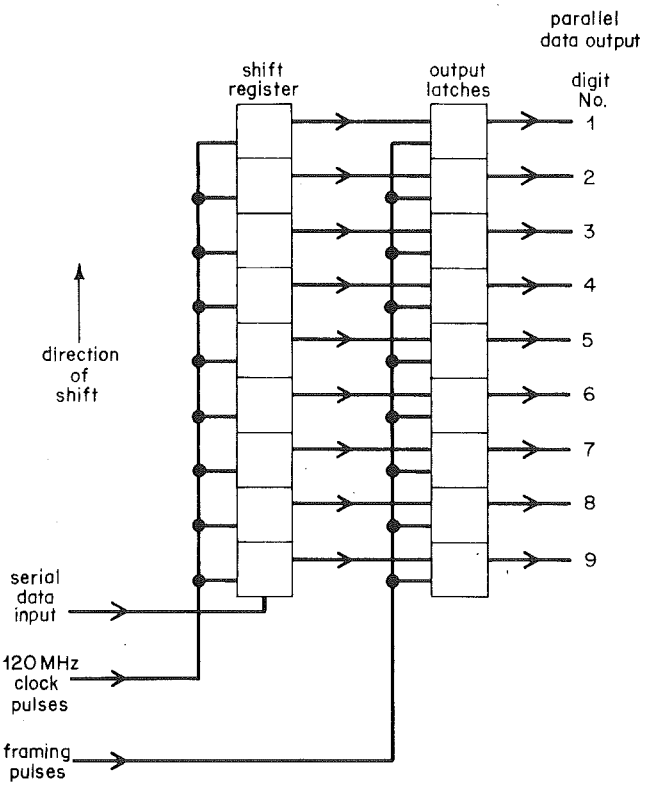

Fig. 3 - Block diagram of the serial-to-parallel converter

The serial data input is clocked into a shift register at 120 MHz. At the instant that the first digit of each word is about to be clocked out of the far end of the shift register, a 13·3 MHz framing pulse triggers the output latches which sample the data in each stage of the shift register, and hold that word until the following one has been shifted up into the shift register, a hold period of approximately 75 ns. The latches thus present the nine digits of each word synchronously on parallel wires to the output.

4. Conclusions

This report has discussed methods by which the parallel digit outputs from a video a.d.c. have been

combined into a single pulse stream suitable for long distance distribution and by which the serial stream is split at the receiving terminal, into the parallel digit streams required by the decoder. Both the sending and receiving units have been built using standard integrated circuits and worked well with little initial setting up.

The design of each unit is capable of being modified easily to meet the exact requirements of a digital video link when the appropriate parameters, such as number of bits per word or clock frequency, are known.

5. References

1. Pulse code modulation of video signals: 8-bit coder and decoder. BBC Research Department Report No. 1970/25.

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